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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/552,701	04/19/2000	Shigemasa Haruhiko	1248-0497P-SP	3009

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Birch Stewart Kolasch & Birch LLP
PO Box 747
Falls Church, VA 22040-0747

EXAMINER	
PUENTE, EMERSON C	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 05/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/552,701	HARUHIKO ET AL.	
	Examiner	Art Unit	
	Emerson C. Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2005* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 10-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8 and 10-22* is/are rejected.

7)☒ Claim(s) *23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1, 3-8, and 10-24 have been examined. Claims 1, 3-8, and 10-22 have been rejected. Claims 23 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. This action is made **Final.**

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 6, 8, 10, 11, 13, and 19-22 are rejected under 35 U.S.C. §**102(b)** as being clearly anticipated by Japanese Patent No. 01-223586 of Omichi et al. referred hereinafter "Omichi".

In regards to claim 1, Omichi discloses a microcomputer having an at least partially built-in nonvolatile memory (see page 6 lines 14-16) including:

a communication circuit for receiving a test program for said nonvolatile memory for an external check system (see figure 1 and page 5);

a RAM on which said test program is run (see item 5 figure 1 and page 9);

a boot ROM comprising a control program (see page 7 lines 1-8) for, upon receiving a test command issued by the external check system, enabling said receiving of said test program from said external check system using said communication circuit (see page 8 lines 7-17) and running of said test program on said RAM (see page 9);

In regards to claim 3, Omichi discloses a microcomputer having an at least partially erasable built-in nonvolatile memory (see page 6 lines 14-16) including:

a nonvolatile memory (see item 4 figure 1);

a boot ROM (see item 4 figure 1);

a RAM (see item 5 figure 1);

a CPU for running a program stored in said boot ROM and RAM (see item 5 figure 1); and

a communication circuit for controlling a communication with a check system (see figure 1), said boot ROM having stored a control program(see page 5-6) for jobs of:

upon receiving a test command issued from said check system, receiving a test program for said nonvolatile memory from said check system to be stored in said RAM (see page see page 8 lines 7-17);

running said test program (see page 9); and

sending a test result to said check system (see page 6).

In regards to claim 4, Omichi discloses a check system of an at least partially erasable built-in nonvolatile memory (see page 6 lines 14-16) in a microcomputer furnished with:

at least one external communication device connected to said microcomputer in such a manner so as to allow a communication in a one-to-one correspondence. Omichi discloses the microcomputer is mounted to a reader/writer (or host computer) and exchanges data with the reader/writer (see page 6);

each external communication device including,

a storage device having a stored a test program for said built-in nonvolatile memory in said microcomputer. Omichi indicates the storage of the operations test program in the testing device (see page 8), and

a communication microcomputer for sending said test program to said microcomputer. It would be inherent for the external device to have a communication microcomputer in order to establish communication with the microcomputer, enabling it to send said test program to said microcomputer.

wherein said microcomputer includes a boot ROM comprising a control program (see page 7 lines 1-8) for, upon receiving a test command issued by the external check system, enabling receiving of said test program from said external check system using said

communication circuit (see page 8 lines 7-17) and running of said test program on said RAM (see page 9).

In regards to claim 6, Omichi discloses a check system of an at least partially erasable built-in nonvolatile memory (see page 6 lines 14-16) in a microcomputer furnished with an external communication device including:

a storage device having stored a test program for said microcomputer having a built-in nonvolatile memory. Omichi indicates the storage of the operations test program in the testing device (see page 8),

a communication control circuit for controlling a communication with said microcomputer. Omichi discloses sending of data blocks from the external device containing mode identification information to determine kind of processing, which constitutes controlling a communication with said microcomputer (see page 7).

a communication microcomputer for sending said test program to said microcomputer when checking the built-in nonvolatile memory therein. It would be inherent for the external device to have a communication microcomputer in order to establish a communication means with microcomputer, enabling it to send said test program to said microcomputer.

wherein said microcomputer includes a boot ROM comprising a control program (see page 7 lines 1-8) for, upon receiving a test command issued by the external check system, enabling receiving of said test program from said external check system using said communication circuit (see page 8 lines 7-17) and running of said test program on said RAM (see page 9).

In regards to claim 8, Omichi discloses the an IC card packing a microcomputer having an at least partially erasable built-in nonvolatile memory (see page 6 lines 14-16) including:

a communication circuit for receiving a test program for a nonvolative memory for an external check system (see figure 1 and page 5) ; and

a RAM on which said test program is run (see item 5 figure 1 and page 9).

a boot ROM comprising a control program see page 7 lines 1-8) for, upon receiving a test command issued by the external check system, enabling receiving of said test program from said external check system using said communication circuit (see page 8 lines 7-17) and running of said test program on said RAM (see page 9).

In regards to claim 10, Omichi discloses an IC card packing a computer having an at least partially erasable built-in nonvolatile memory (see page 6 lines 14-16) including:

said at least partially erasable nonvolatile memory (see item 4 figure 1 and page 1 lines 14-16);

a boot ROM (see item 4 figure 1);

a RAM (see item 5 figure 1);

a CPU for running a program stored in said boot ROM and RAM (see figure 1); and

a communication circuit for controlling a communication with a check system (see figure 1),

said boot ROM having stored a control program (see page 5-6) for jobs of:

upon receiving a test command issued from said check system, receiving a test program for said nonvolatile memory from said check system to be stored in said RAM (see page 8 lines 7-17)

running said test program (see page 9); and

sending a test result to said check system (see page 6)

In regards to claim 11, Omichi discloses a check system of an IC card packing a microcomputer having an at least partially erasable built-in nonvolatile memory (see page 6 lines 14-16) furnished with:

at least one external communication device connected to said microcomputer packed in said IC card in such a manner so as to allow a communication in a one-to-one correspondence. Omichi discloses the IC card mounted to a reader/writer (or host computer) and exchanges data with the reader/writer (see page 6);

each external communication device including,

a storage device having a stored a test program for said built-in nonvolatile memory in said microcomputer. Omichi indicates the storage of the operations test program in the testing device (see page 8), and

a communication microcomputer for sending said test program to said IC card. It would be inherent for the external device to have a communication microcomputer in order to establish a communication means with IC card, enabling it to send said test program to said IC card.

wherein said microcomputer includes a boot ROM comprising a control program see page 7 lines 1-8) for, upon receiving a test command issued by the external check system, enabling receiving of said test program from said external check system using said communication circuit (see page 8 lines 7-17) and running of said test program on said RAM (see page 9).

In regards to claim 13, Omichi discloses a check system of an IC card packing a microcomputer having an at least partially erasable built-in nonvolatile memory (see page 6 lines 14-16) furnished with an external communication device including:

a storage device having stored a test program for a built-in nonvolatile memory in said microcomputer packed in said IC card. Omichi indicates the storage of the operations test program in the testing device (see page 8),

a communication control circuit for controlling a communication with said IC card. Omichi discloses sending of data blocks from the external device containing mode identification information to determine kind of processing, which constitutes controlling a communication with said IC card(see page 7).

a communication microcomputer for sending said test program to said IC card when checking the built-in nonvolatile memory therein. It would be inherent for the external device to have a communication microcomputer in order to establish a communication means with the IC card, enabling it to send said test program to said IC card.

wherein said microcomputer includes a boot ROM comprising a control program (see page 7 lines 1-8) for, upon receiving a test command issued by the external check system, enabling receiving of said test program from said external check system using said

communication circuit (see page 8 lines 7-17) and running of said test program on said RAM (see page 9).

In regards to claim 19-22, Omichi discloses wherein enabling said receiving of said test program performed by the control program of said boot ROM comprises allocating an area on said RAM sufficient to receive the test program and controlling said communication circuit to receive and transmit the test program to said RAM (see page 8 lines 7-17).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 7, 12, and 14-18, are rejected under 35 U.S.C. § **103(a)** as being unpatentable over Omichi in further view of US Patent No 5,818,848 of Lin et al. referred hereinafter "Lin".

In regards to claim 5 and 7, Omichi teaches all claimed subjected matter, as stated above, except a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of microcomputers each having a built-in nonvolatile memory and connected to said plurality of external communication devices, respectively.

However, Lin discloses a check system comprising of a control computer connected to a plurality of integrated circuits comprising of a test circuitry, for intensively control a check-up of a plurality of integrated circuits (see figure 2 and column 2 lines 21-25 and column 4 lines 60-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Omichi to incorporate a check system including a control computer, connected to a plurality of external communication devices, for intensively controlling

a check-up of a plurality of microcomputers each having a built-in nonvolatile memory and connected to said plurality of external communication devices, respectively. A person of ordinary skill in the art would have been motivated to make the modification to Omichi because Omichi discloses the testing of microcomputers and having a control computer, connected to a plurality of integrated circuits or external communication devices which are connected to a corresponding microcomputer, as per teaching of Lin, would provide for an more efficient means of testing of microcomputers.

In regards to claim 12 and 14, Omichi teaches all claimed subjected matter, as stated above, except a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of IC cards connected to said plurality of external communication devices, respectively.

However, Lin discloses a check system, which comprises a control computer connected to a plurality of integrated circuits comprising of a test circuitry, for intensively control a check-up of a plurality of integrated circuits (see figure 2 and column 2 lines 21-25 and column 4 lines 60-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Omichi to incorporate a check system including a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of IC cards connected to said plurality of external communication devices, respectively. A person of ordinary skill in the art would have been motivated to make the modification to Omichi because Omichi discloses the testing of an IC card and having a control computer, connected to a plurality of integrated circuits or external communication devices which are connected to a corresponding IC card, as per teaching of Lin, would provide for an more efficient means of testing of IC cards.

In regards to claim 15 and 16, Omichi teaches all claimed subjected matter, as stated above, except a plurality of microcomputers each having a built-in volatile memory, and wherein said check system comprises a control computer connected to a plurality of external communication devices, for intensively controlling a check-up of said plurality of

microcomputers each connected to said plurality of external communication devices, respectively.

However, Lin discloses a check system which comprises a control computer connected to a plurality of external communication devices comprising of a test circuitry, for intensively control a check-up of said microcomputers (see figure 2 and column 2 lines 21-25 and column 4 lines 60-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Omichi to incorporate a check system including a control computer, connected to a plurality of external communication devices, for intensively controlling a check-up of a plurality of IC cards connected to said plurality of external communication devices, respectively. A person of ordinary skill in the art would have been motivated to make the modification to Omichi because Omichi discloses the testing of an IC card and having a control computer, connected to a plurality of integrated circuits or external communication devices which are connected to a corresponding IC card, as per teaching of Lin, would provide for an more efficient means of testing of IC cards.

Furthermore, Omichi discloses a microcomputer including a boot ROM comprising a control program for enabling receiving of said test program through a communication circuit and running of said test program on said RAM (see pages 8-9) and Lin discloses testing a plurality of integrated circuits or microcomputers in response to receiving test commands issued by the control computer (see figure 2 and column 2 lines 21-25 and column 4 lines 60-67), thus indicating each of said plurality of microcomputers including a boot ROM comprising a control program for enabling receiving of said test program through a communication circuit in response to receiving a test command issued by the control computer and running of said test program on said RAM.

In regards to claim 17 and 18, Omichi discloses a microcomputer including a boot ROM comprising a control program for enabling receiving of said test program through a communication circuit and running of said test program on said RAM (see page 5-9), and Lin discloses testing a plurality of integrated circuits or microcomputers in response to receiving test commands issued by the control computer (see figure 2 and column 2 lines 21-25 and column 4

lines 60-67), thus indicating each of said plurality of microcomputers including a boot ROM comprising a control program for enabling receiving of said test program through a communication circuit in response to receiving a test command issued by the control computer and running of said test program on said RAM.

Allowable Subject Matter

Claim 23 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

Applicant's arguments filed March 16, 2005 have been fully considered but they are not deemed to be persuasive.

In regards to applicant's argument "In the present invention, the boot ROM contains a control program for enabling receiving of the test program from an external check system upon receiving a test command issued by the external check system. The test program is for the nonvolatile memory of the microcomputer. In order to make this distinction clear, applicant have amended claim 1 to indicate that the nonvolatile memory, unlike the boot ROM is 'an at least partially erasable built-in nonvolatile memory.' Applicant submits that Omichi's ROM 4 does not teach both a boot memory." Applicants submit that Omichi's ROM 4 does not teach both a boot ROM comprising a control program for enabling receiving the test program for a nonvolatile memory and the at least partially erasable built-in memory that is the subject of the testing by the test program," (see page 11 and 12 under remarks) examiner respectfully disagrees. Examiner maintains his rejection.

Omichi disclose the ROM including mask ROM, PROM, and EEPROM (electrically erasable ROM), thus indicating partially erasable built in nonvolatile memory (see page 6).

In regards to arguments of Omichi in view of Chan and Omichi in view of Chan and Lin, arguments moot in view of new grounds of rejection.

In response to applicant argument "New claims 19-22 further define the function of 'receiving' as comprising allocating an area on the RAM sufficient to receive the test program,

which is based on the disclosure at page 24 of the present specification. Applicant submit that Omichi, Chan, and Lin, either alone or in combination, fails to teach or suggest at least the limitation expressed in new claims 19-22)," examiner respectfully disagrees. Omichi dislcoses allocating an area on the RAM sufficient to receive the test program (see page 8 lines 12-17).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Omichi discloses the a boot ROM comprising a control program for enabling receiving of said test program through a communication circuit in response to receiving a test command issued by the external check system and Lin discloses the teaching of testing the plurality of integrated circuits microcomputers with a control computer, thus indicating the limitations set forth. Examiner maintains rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C. Puente whose telephone number is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Emerson Puente
5/5/05

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100